PROGRAMMABLE PHASE SHIFT CIRCUITRY

ABSTRACT OF THE DISCLOSURE

A circuit provides a programmable phase shift feature, where the phase shift is programmably selectable by a user. This circuitry may be incorporated in a programmable logic device (PLD) or field programmable gate array (FPGA) to provide additional programmability features. The programmable phase shift circuitry may be implemented within a phase locked loop (PLL) or delay locked loop (DLL) circuit.

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